Notice of Allowability	Application No.	Applicant(s)	
	09/940,299	WENDORF ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 05/22/2006*.

2. ☒ The allowed claim(s) is/are *1,3,5-7,9,12-16,18-21,23,26-30,34-37,40-44,47,48 and 54-57*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1, 3, 5-7, 9, 12-16, 18-21, 23, 26-30, 34-37, 40-44, 47,48 and 54-57 are pending in the current application and have been examined.

Response to Arguments

2. Applicant's arguments, filed 05/22/2006, with respect to independent claims 1, 16, 30 and 44 have been fully considered and are persuasive. Further, in light of the Examiner's Amendment listed below the Rejection of the Previous Office Action of Record has been withdrawn.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Farad E. Amini on 08/03/2006.

The application has been amended as follows:

Claim 1:

Please amend claim 1 as follows:

On line 6, change "first memory testing" to "first memory testing engine".

On line 11, change "second MTE is embedded" to "second MTE is integrated".

On line 20, change "if data traffic" to "if normal data traffic".

Claim 16:

Please amend claim 16 as follows:

Change line 7 from "accessing from the processor through the bus the plurality of random access" to "accessing from the processor through the bus normal data traffic to and from the plurality of random access".

Claim 30:

Please amend claim 30 as follows:

On line 3, change "accessing over a bus" to "accessing over a bus normal data traffic to and from".

Claim 44:

Please amend claim 44 as follows:

On line 14, change "passing data traffic" to "passing normal data traffic".

Allowable Subject Matter

Claims 1, 3, 5-7, 9, 12-16, 18-21, 23, 26-30, 34-37, 40-44, 47,48 and 54-57 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to testing random access memory (RAM) devices.

The claimed invention as set forth in **claim 1** recites features such as:

A system, which comprises:

a bus;

a first random access memory (RAM);

a first memory testing engine (MTE) to execute test operations on the first random access memory;

a first bus controller for the bus, and in which the first memory testing engine is integrated to have a first memory interface which is shared with the first memory testing engine to access the first RAM;

a second RAM;

a second MTE to execute test operations on the second RAM;

a second bus controller for the bus, and in which the second MTE is integrated to have a second memory interface which is shared with the second MTE to access the second RAM; and

a processor; and.

wherein each bus controller is to provide the processor access to random access memory via its respective memory interface, and the processor is to control each memory testing engine via the bus and the respective bus controller and wherein each memory testing engine uses data, address and control pathways used by its respective bus controller so that if normal data traffic from the processor is being passed to a memory module by the respective bus controller, its integrated memory testing engine cannot run a test function.

The prior arts of record teach the claimed bus, first RAM, first MTE, first bus controller and processor. The prior arts of record also teach separate interfaces within the microprocessor, to access the memories 510. The external test controller 580 only

uses the test management logic 570 (interface) to access the memories 510 via test bus 575, whereas normal peripheral circuits only use the bus unit 530 (a different interface) to access the same memories 510 via normal bus 554 (a different bus); Miner (US-6370661) is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, that the testing functions by the MTE, as well as non-testing functions or "normal data traffic" by the processor, be performed upon the associated memory using the **same** memory interface and the **same** bus since the MTE shares the same memory interface and the same bus as its respective bus controller.

As such, modification of the prior art of record to include the claimed *utilization of the same memory interface and bus for both testing and non-testing (normal data traffic) functions* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *utilization of the same memory interface and bus for both testing and non-testing (normal data traffic) functions* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *utilization of the same memory interface and bus for both testing and non-testing (normal data traffic) functions* as set forth in **claim 1**. **Claim 44** recites similar allowable features as in **claim 1** and is allowable for the same reasons as set forth for **claim 1**.

The claimed invention as set forth in **claim 16** recites features such as:

A method which comprises:

transmitting a plurality of initiation signals from a processor via a bus to a plurality of memory testing engines via a plurality of bus controllers, respectively, for the bus;

testing a plurality of random access memories, respectively, using the plurality of initiated memory testing engines, respectively;

accessing from the processor through the bus normal data traffic to and from the plurality of random access memories via the plurality of bus controllers, respectively;

accessing from the bus controllers the random access memories using a plurality of memory controllers, respectively; and

passing control of data, address and control pathways between (1) each one of the memory test engines, and (2) a respective one of the bus controllers, so that only one of the two has control at one time.

The prior arts of record teach transmitting a plurality of initiation signals (testing parameters) from a processor (external test controller 580) via a bus (test bus 575) to a **single** memory testing engine (test management logic 570) via a **single** bus controller (bus unit 530) and testing a plurality of random access memories (memories 510), respectively, using the **single** initiated memory testing engine". The prior arts of record also teach passing control of data, address and control pathways between the memory test engine (test management logic 570) and the bus controller (bus unit 530), so that only one of the two has control at one time. The prior arts of record further teach

separate interfaces within the microprocessor, to access the memories 510. The external test controller 580 only uses the test management logic 570 (interface) to access the memories 510 via test bus 575, whereas normal peripheral circuits only use the bus unit 530 (a different interface) to access the same memories 510 via normal bus 554 (a different bus); Miner (US-6370661) is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, "accessing from the processor through the bus normal data traffic to and from the plurality of random access memories via the plurality of bus controllers". In other words, the **same** bus is used to pass **both** normal data traffic and test traffic to the memories using each of a number of bus controllers for the **same** bus.

As such, modification of the prior art of record to include the claimed *utilization of the same bus for both testing and non-testing (normal data traffic) functions* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *utilization of the same bus for both testing and non-testing (normal data traffic) functions* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *utilization of the same bus for both testing and non-testing (normal data traffic) functions* as set forth in **claim 16**. **Claim 30** recites similar allowable features such as, "accessing over a bus normal data traffic to and from each of a plurality of memories that is associated with a respective one of a plurality of ASICs, via a respective one of a

plurality of utility bus slave (UBS) controllers on the respective ASIC", as in **claim 16** and is allowable for the same reasons as set forth for **claim 16**. Hence, claims 1, 3, 5-7, 9, 12-16, 18-21, 23, 26-30, 34-37, 40-44, 47,48 and 54-57 are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefore, the Examiner favors the allowance of claims 1, 3, 5-7, 9, 12-16, 18-21, 23, 26-30, 34-37, 40-44, 47,48 and 54-57. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 8/4/06

John J. Tabone, Jr.
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER